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DELIVER TO: Examiner Patrick G. Wamsley, Art Unit 2819

COMPANY: United States Patent and Trademark Office

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FROM: Alessandro Steinfl

DATE: August 2, 2005

TOTAL NO. OF PAGES (INCLUDING THIS PAGE): 9

SUBJECT : Amendment
U.S. Application No. 10/763,071
Applicant: Todd Kaplan
"Clocked D/A Converter"
Our Ref: 620354-1/AS

REMARKS:

Examiner Wamsley:

Enclosed is a response to the Office Action mailed on May 2, 2005 consisting of:
Response – 8 pages

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Todd Kaplan	Group Art No.: 2819
Application No: 10/763,071	Examiner: Wamsley, Patrick G
Filed: January 21, 2004	Re: **AMENDMENT**
For: "CLOCKED D/A CONVERTER"	Our Ref: B-4850 620354-1/AS
	Date: August 2, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is filed in response to the Official Action dated May 2, 2005, a reply to which is initially due by August 2, 2005. Please enter the following amendments and consider the following remarks with respect to the subject application. All amendments and remarks herein are made without prejudice.

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

* * *

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (original) A digital-to-analog converter comprising:

a differential transistor pair comprising a first input/output transistor and a second input/output transistor, the first input/output transistor and the second input/output transistor having an input terminal, an output terminal and a third terminal, the differential transistor pair receiving a differential logic signal at the input terminals of the first input/output transistor and the second input/output transistor;

a bistable circuit connected with the output terminal of the first input/output transistor and the output terminal of the second input/output transistor;

a clock circuit comprising a first clock transistor and a second clock transistor connected as a differential pair, the first clock transistor and the second clock transistor having a clock input terminal, a clock second terminal, and a clock third terminal, the clock second terminal of the first clock transistor being connected with the third terminal of the first and second input/output transistor, and the clock second terminal of the second clock transistor being connected with the bistable circuit; and

a current source connected with the clock third terminal of the first clock transistor and the clock third terminal of the second clock transistor, wherein:

the clock circuit acts as a switch, controlling the converter so as to provide current from the current source either to the differential transistor pair or to the bistable circuit; and

the input terminals of the first and second input/output transistor receive signals switching between a first logic value and a second logic value, switching between the first logic value and the second logic value occurring when the clock circuit controls the converter so as to provide current from the current source to the bistable circuit, said switching being asserted at the output terminal of the first and second

input/output transistor when the clock circuit controls the converter so as to provide current from the current source to the differential transistor pair.

2. (original) The converter of claim 1, wherein the first logic value and the second logic value of the signals received by the input terminals of the first and second input/output transistor are voltage values and output values of the output terminals of the first and second input/output transistor are current values.

3. (original) The converter of claim 1, further comprising a first resistor connected with the output terminal of the first input/output transistor and a second resistor connected with the output terminal of the second input/output transistor.

4. (original) The converter of claim 3, further comprising a cascode circuit connected with the first and second resistor.

5. (original) The converter of claim 1, wherein the first input/output transistor, second input/output transistor, first clock transistor, and second clock transistor are selected from the group comprising npn transistors, pnp transistors, FET transistors, nMOS transistors, pMOS transistors, CMOS transistors, and MEMS switches.

6. (original) The converter of claim 1, wherein the bistable circuit comprises a first bistable circuit transistor and a second bistable circuit transistor connected as a differential pair, the first and second bistable circuit transistor comprising a bistable circuit first terminal, a bistable circuit second terminal, and a bistable circuit third terminal.

7. (original) The converter of claim 6, wherein the bistable circuit first terminal of the first bistable circuit transistor and the bistable circuit second terminal of the second bistable circuit transistor are connected with the output terminal of the second input/output transistor and the bistable circuit first terminal of the second bistable circuit transistor and the bistable circuit second terminal of the first bistable circuit

transistor are connected with the output terminal of the first input/output transistor, and the bistable circuit third terminal of the first and second bistable circuit transistor are connected with the second clock transistor.

8. (original) A digital-to-analog conversion method comprising:

connecting a first transistor and a second transistor as a differential pair, the first transistor and the second transistor having a switch input terminal, a switch output terminal and a switch third terminal, the first transistor and second transistor receiving a differential logic signal at the switch input terminals;

connecting a bistable circuit with the switch output terminal of the first transistor and the output terminal of the second transistor;

connecting a third transistor and a fourth transistor as a differential pair, the third transistor and the fourth transistor having a clock input terminal, a clock second terminal, and a clock third terminal;

connecting the clock second terminal of the third transistor with the switch third terminal of the first and second transistor;

connecting the clock second terminal of the fourth transistor with the bistable circuit;

connecting the clock third terminal of the third transistor and fourth transistor with a current source;

providing the switch input terminal of the first transistor with a first input signal and the switch input terminal of the second transistor with a second input signal complementary to the first input signal, the first and second input signals being switchable between a first logic input value and a second logic input value;

providing the clock input terminal of the third transistor with a first clock signal and the clock input terminal of the fourth transistor with a second clock signal complementary to the first clock signal; and

switching the first clock signal between a first clock value and a second clock value, the first clock value allowing the third transistor to conduct current from the current source to the first and second transistor and allowing the fourth transistor to block current from the current source to the bistable circuit, the second clock value

allowing the third transistor to block current from the current source to the first and second transistor and allowing the fourth transistor to conduct current from the current source to the bistable circuit.

9. (original) The method of claim 8, wherein the differential logic signal at the input terminals of the first and second transistor comprises an input signal switching between a first logic value and a second logic value.

10. (original) The method of claim 9, wherein switching between the first logic value and the second logic value occurs during the second clock value of the first clock signal.

11. (original) The method of claim 10, wherein said switching is asserted at the switch third terminal of the first and second transistor during the first clock value of the first clock signal.

12. (original) A digital-to-analog converter comprising:

an input /output circuit receiving a digital input signal and outputting an analog output signal;

a bistable circuit connected with the input /output circuit;

a clock circuit connected with the input/output circuit and the bistable circuit; and

a current generator circuit connected with the clock circuit, wherein:

the clock circuit acts as a switch, providing current from the current generator either to the input/output circuit or to the bistable circuit;

the digital input signal is a switchable signal switching when the current generator provides current to the bistable circuit ; and

the analog output signal is a switchable signal associated with the digital input signal, the analog output signal switching when the current generator provides current to the input/output circuit.

13. (original) The converter of claim 12, further comprising a cascode circuit connected with the input/output circuit.

14. (currently amended) A non-return-to-zero digital-to-analog converter comprising a single current source and having a first input, a second input and an output, wherein the first input determines how current is routed between the current source and the output, and the second input determines when routing of the current between the current source and the output is allowed to change , wherein the first input is a digital voltage input and the output is an analog current output.

15. (original) The digital-to-analog converter of claim 14, wherein the second input is a clock signal.

16. (canceled) ~~The digital-to-analog converter of claim 14, wherein the first input is a digital voltage input and the output is an analog current output.~~

* * *

REMARKS

Amendments to the claims

Claims 1-16 are pending in the application. Claim 14 has been amended to incorporate the features of claim 16. Claim 16 has been canceled without prejudice. No new matter has been added.

Claim Rejections – 35 USC § 103

In the Action, the Examiner rejects claims 14-16 under 35 USC § 103(a) as being unpatentable over the Admitted Prior Art (APA), in view of U.S. Pat. No. 6,597,303 to Cosand. The Applicant respectfully disagrees.

Claim 14 as amended recites *"[a] non-return-to-zero digital-to-analog converter . . . having a first input, a second input and an output . . . wherein the first input is a digital voltage input and the output is an analog current output"* (emphasis added). According to the Examiner, such feature is disclosed in Cosand, column 2, lines 16-24. That passage of Cosand makes reference to Figure 1 of Cosand. However, with reference to Figure 1 of Cosand, although a current signal is output at the collectors of Q1 and Q2, the output of the circuit of Figure 1 in Cosand is read at nodes A and B, and that output is a voltage digital signal, as also stated on column 2, lines 22-24 of Cosand (. . . a voltage difference . . . which is an amplified replica of the input voltage difference at the bases of Q1 and Q2) and not *"an analog current output"* as recited in claim 14 as amended.

In view of the above, the Applicant submits that the Examiner is not in a condition to make a prima facie 35 USC § 103 case against claim 14. Therefore, claim 14 is patentable over APA and Cosand, together with claim 15, at least by virtue of its dependence on claim 14.

Allowable subject matter

The Examiner states that claims 1-13 are allowed. The Applicant thanks the Examiner for the indication of allowability of those claims.

The Applicant submits that all claims of the application as amended herein are in condition for allowance. Prompt issuance of a Notice of Allowance is earnestly solicited.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, fax no. (571)-273-8300 on

August 2, 2005
(Date of Deposit)

Susan Papp
(Name of Person Depositing)

Susan Papp
Signature

08/02/05
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Respectfully submitted,

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